ABSTRACT

A method and apparatus are provided for reducing leakage current in a read only memory device. Leakage current is reduced by applying a biased gate voltage (relative to a source voltage) to the gate of at least one of transistor in the array. The biased gate voltage is applied at least during a precharge phase of a read cycle. When the array transistors are n-channel transistors, the biased voltage is a negative bias voltage (relative to the source voltage). When the array transistors are p-channel transistors, the biased voltage is a positive bias voltage (relative to the source voltage). Applying a negative backgate bias to the transistor's p-well contact can also reduce n-channel transistor subthreshold leakage current. Thus, for an n-channel array, a negative gate voltage and backgate bias (optional) are applied to cell transistors in the off state. Similarly, the subthreshold leakage current of p-channel transistors is reduced by applying a more positive gate-to-source bias and a positive n-well-to-source bias.

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